**Student Paper**

# 80nm $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InAs_{0.3}P_{0.7}$ Composite Channel HEMT with an $f_T$ of 280GHz

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InAlAs/InGaAs high electron mobility transistors (HEMTs) have shown excellent performance for high speed and low noise applications. However, due to the small band gap of InGaAs channel layer, these devices suffer from strong impact ionization in the channel. It has been demonstrated that using a composite channel structure is an effective way to improve the frequency performance, breakdown characteristics, and output power of the InAlAs/InGaAs HEMTs as the result of larger bandgap, higher electron saturation velocity in the composite channel [1]. Even though InP is the material mostly studied, InAsP is an excellent candidate for the sub-channel because it has smaller conduction band offset with InGaAs than InP. So electrons can be more easily transferred into the InAsP sub-channel. In this paper, we present an 80nm $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InAs_{0.3}P_{0.7}$ HEMT with a cut-off frequency ($f_T$) of 280 GHz, which is, to our knowledge, the highest ever reported for this type of InP-based composite channel HEMTs.

The device structure (Figure 1) used in this study was grown by Molecular Beam Epitaxy on the Fe-doped semi-insulating (100) InP substrate. For device processing, the active area was first isolated by dry mesa etching with $Cl_2$/Ar plasma in an inductively coupled plasma reactive ion etching system. After Ge/Au/Ni/Au ohmic contact, mushroom-shaped gates were patterned by electron beam lithography using ZEP520A/PMGI/ZEP520A tri-layer resists. For gate recess, citric acid/$H_2O_2$ mixture and Ar plasma were used to etch InGaAs and InP respectively. The DC characteristics of a typical composite channel HEMT is shown in Figure 2. The device exhibited a maximum current of 610mA/mm at a gate voltage ($V_{gs}$) of 0.2 V and a drain voltage ($V_{ds}$) of 1 V. The device is well pinched off at a gate bias of –0.65 V. As shown in Figure 3, the maximum extrinsic transconductance ($g_m$) achieved is 1 S/mm at $V_{gs}$ = -0.19 V and $V_{ds}$ = 1 V. The threshold voltage, obtained by extrapolating the linear region of $I_d$ versus $V_{gs}$ curve from the $V_{gs}$ of maximum $g_m$, is - 0.48 V. The on-state gate leakage current is measured and shown in Figure 4. The typical bell-shaped $I_{gs}$ curve, a sign of impact ionization, is not shown up to $V_{ds}$ = 1.5 V, which proves that using InAsP as the composite channel successfully suppresses the impact ionization process in $In_{0.53}Ga_{0.47}As$ layer.

The small signal microwave characteristics of the composite channel HEMT were measured using an Agilent 8510C network analyzer from 1 GHz to 50 GHz. Figure 5 shows the frequency dependence of current gain and maximum available/stable gain when the HEMT is biased at $V_{gs}$= - 0.14 V and $V_{ds}$ = 1.0 V. By extrapolating the gains at –20dB/dec slope with least square fitting, the $f_T$ and maximum frequency of oscillation ($f_{max}$) are determined to be 280 GHz and 184 GHz, respectively. The $f_T$, $f_{max}$ and total delay time ($1/2\pi f_T$) is plotted as a function of the reciprocal of drain current in Figure 6. The device exhibited a high $f_T$ of more than 200GHz in a wide gate bias range. Combined with previous results, the gate length dependence of $f_T$ and $f_{max}$ is plotted in Figure 7 [2]. By down-scaling the gate length, the high frequency performances of the composite channel HEMTs are comparable to the reported best devices of conventional InAlAs/InGaAs HEMTs with the same gate length.

In conclusion, we have demonstrated a high performance 80nm gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InAs_{0.3}P_{0.7}$ composite channel HEMT. The device has a $g_m$ as high as 1 S/mm and an $f_T$ of 280 GHz. To complete this study, the noise and power performance of such device will be further studied and compared with conventional InGaAs channel devices in near future.

**Reference**

[1]. T. Enoki, K. Arai, A. Kohzen and Y. Ishii, "InGaAs/InP double channel HEMT on InP," *Proc. 4th IPRM Conf.,* 1992, pp. 14 – 17.

[2]. D. Liu, M. Hudait, Y. Lin, H. Kim, S. A. Ringel, W. Lu, "Gate length scaling study of InAlAs/InGaAs/InAsP composite channel HEMTs", Solid State Electronics, 51, 6, p. 838-841



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| | | | |
|---|---|---|---|
| Cap | $n^+$InGaAs | 400Å | $1x10^{19}$ $cm^{-3}$ |
| EtchingStop | InP | 60Å | Undoped |
| Barrier | InAlAs | 100Å | Undoped |
| δ-doping | Si | - | $6x10^{12}$ $cm^{-2}$ |
| Spacer | InAlAs | 30Å | Undoped |
| Channel | InGaAs | 70Å | Undoped |
| Channel | InAsP | 40Å | Undoped |
| Channel | $n^-$InAsP | 40Å | $2x10^{18}$ $cm^{-3}$ |
| Buffer | InAlAs with supperlattice | 3600Å | Undoped |
| Substrate | InP | - | - |

Figure 1. MBE-grown layer structure for InAlAs/InGaAs /InAsP composite channel HEMT on InP substrate.

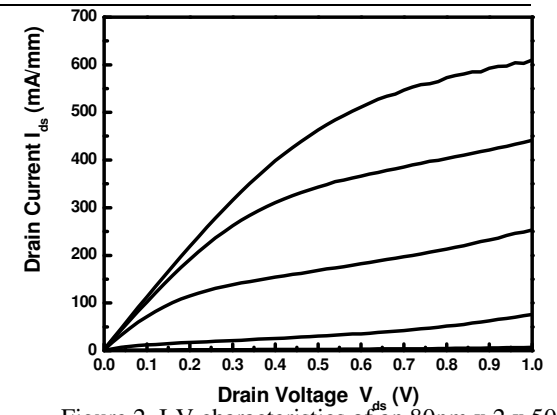


Figure 2. I-V characteristics of an 80nm x 2 x 50 µm composite channel HEMT. The gate is biased from –0.6 V to 0.2 V at a step of 0.2 V.

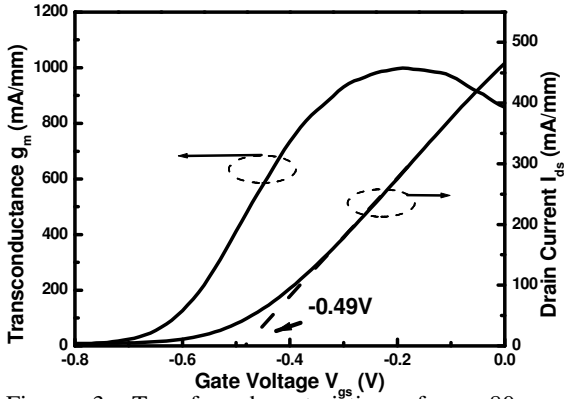


Figure 3. Transfer characteristics of an 80nm composite channel HEMT.The drain is biased at 1 V.

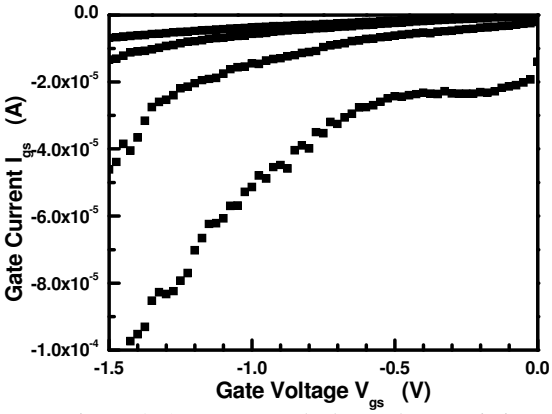


Figure 4. On state gate leakage characteristics of an 80nm composite channel HEMT. The drain is biased from 0 to 1.5 V at a step of 0.5 V.

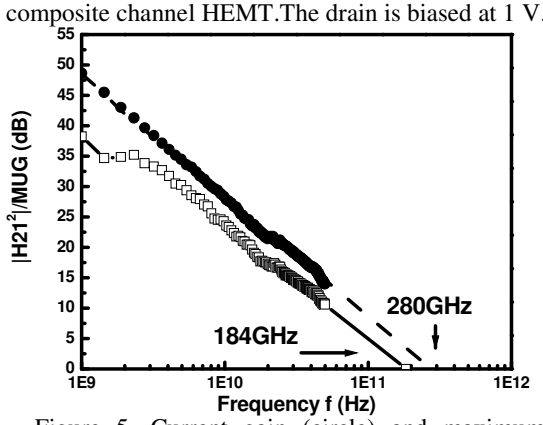


Figure 5. Current gain (circle) and maximum unilateral gain (rectangular) characteristics of a 80nm composite channel HEMT.

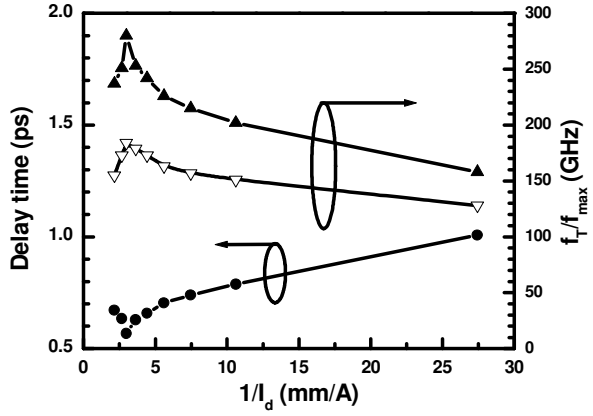


Figure 6. $f_T$(triangle)/$f_{max}$(rectangular) and total delay time (circle) as a function of the reciprocal of drain current density for a 80nm composite channel HEMT.

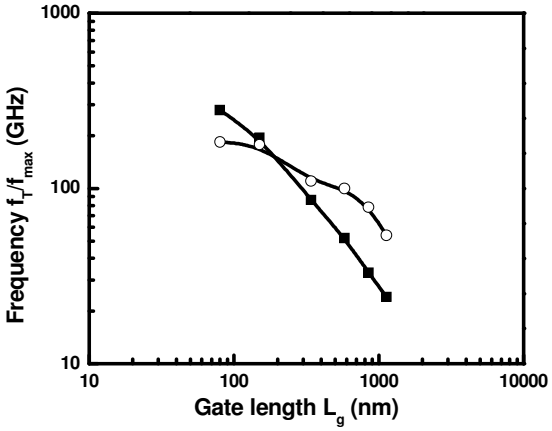


Figure 7. The dependence of $f_T$ (rectangular) and $f_{max}$ (circle) on gate length.